Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1-7. (Cancelled)

8. (Currently Amended) Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, the circuit comprising:

a first and a second asynchronous clock domain, wherein jitter elements are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain.

9. (Cancelled)

10. (Currently Amended) The system of claim 8, wherein the at least one of the jitter elements comprise delay elements for introducing predetermined timing delays which are randomly exercised.

11. (Currently Amended) The system of claim 8, wherein the at least one of the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

12. (Currently Amended) The system of claim 8, wherein the at least one of the jitter elements are interactively inserted by a user.

13. (Currently Amended) The system of claim 8, wherein the at least one of the jitter elements are automatically inserted using predetermined modules.

14-15. (Cancelled)